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EXAMINER	
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ART UNIT	PAPER NUMBER
2187	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/538,371	DUTTA, SANTANU	
	Examiner	Art Unit	
	KALPIT PARIKH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9,11-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,11-14, and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant detailed action is in response to Applicant's submission filed on 17 July 2008.

I. APPLICATION INFORMATION

Application No. 10/538371 has a total of 13 claims pending in the application; there are 3 independent claims and 10 dependent claims, all of which are ready for examination by the examiner.

II. REJECTIONS NOT BASED ON PRIOR ART

Claim Objection

CLAIM 1 recites 'to provide circular-access for each set of one or more buffers such that an access to the last position in a particular set of one or more buffers.' It appears the claim language is incomplete because no result is recited to correspond to the 'such that.'

CLAIM 1 recites 'each buffer of the plurality of independent buffers.' It appears the claim may more clearly recite the subject matter if it were to instead recite each independent buffer of the planarity of independent buffers.

CLAIM 7 recites each buffer of the plurality of independent buffers. It appears the claim may more clearly recite the subject matter if it were to instead recite each independent buffer of the planarity of independent buffers.

CLAIM 4 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 1 recites the sets of buffers matched to respective ones of a plurality of source-destination paths. Claim 4 recites the controller is configured to allocate the plurality of

independent buffers among a plurality of sour-destination paths. It is unclear how claim 4 further limits claim 1 because the sets of buffers correspond to the plurality of independent buffers.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **CLAIMS 1-4, 6-9, 11-14, 16** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

   Claim 1 recites a controller configured to configure the plurality of independent buffers into sets of buffers. It is unclear if the limitation is to be taken to mean the plurality of independent buffers are configured to form sets of buffers (i.e., each set of buffers comprises a plurality of independent buffers) or the plurality independent buffers are each further partitioned into sets of buffers. The ambiguity creates further confusion in other parts of the claim.

   Claim 1 recites 'a select buffer of the plurality of independent buffers.' It is unclear if the select buffer is to be taken as an independent buffer or a buffer of an independent buffer.

   Claim 2 recites 'a select buffer of the plurality of independent buffers.' Claim 1 recites 'a select buffer of the plurality of independent buffers.' It is unclear if the two instances of 'a select buffer' are intended to recite to the same or different claim elements.

   Claim 2 recites 'a bit-overwrite function that overwrites bits of the address that differentiate the select buffer from others of the plurality of independent buffers while not overwriting bits that indicate the location within the select buffer.' During an increment operation bits are understood to be overwritten. For example when a pointer is incremented from '00' to '01' one of the bits is overwritten

from '0' to '1.' It is unclear how a circular increment function can be implemented without performing an overwrite of the bits that indicate the locations within the select buffer as apparently recited in the claims. For purposes of examination the explanation presented in page 10 lines 21-32 of the specification was relied upon to ascertain the intended meaning of the claim.

Claim 2 recites 'the select buffer.' Claim 1 and claim 2 each separately recite 'a select buffer.' It is unclear which select buffer is being referenced.

Claim 7 recites 'partition the plurality of independent buffers into sets of buffers.' It is unclear if the limitation is to be taken to mean the plurality of independent buffers are partitioned sets of independent buffers (i.e., each set comprises a plurality of independent buffers) or the plurality independent buffers are each further partitioned into sets of buffers. The ambiguity creates further confusion in the limitation 'each set of the sets of one or more buffers and wherein at least one set of the sets of one or more buffers has two or more buffers.'

Claim 9 recites 'the buffer within the buffer memory.' It is unclear which buffer is being reference, an independent buffer or a buffer of the sets of buffers.

Claim 11 recites a controller configured to configure the plurality of independent buffers into sets of one or more of the independent buffers. It is unclear if the limitation is to be taken to mean the plurality of independent buffers are configured to form sets of buffers (i.e., each set comprises a plurality of independent buffers) or the plurality independent buffers are each further partitioned into sets of buffers.

Claim 11 recites 'to configure the plurality independent buffers into sets of one or more of the independent buffers.' The claim does not previously recite 'a plurality of independent buffers.' It is unclear if 'the plurality of independent buffers' refers to 'a plurality of buffers.'

Claim 11 recites 'wherein at least one set of the sets of buffers has two or more buffers.' It is unclear if the 'two or more buffers' are two or more of the plurality of independent buffers or some other buffers.

Claim 14 recites 'the buffer.' It is unclear which buffer is being reference, an independent buffer or a buffer of the sets of buffers.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **CLAIMS 1, 3-4, 7-9, AND 12-14** rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway et al. (US PGPUB No. 20030061269) in view of Nogradi (US Pat No. 5947518).

As per claim 1, Hathaway et al. disclose a buffer management system for providing a plurality of independent buffers for use by an application (see FIG 2: 220), the system comprising:

- a buffer memory (see Hathaway et al. FIG 1: 250: Object Memory), and
- a controller operably coupled to the buffer memory (see Hathaway et al. PAGE 3 [0053]: "an OMU (such as OMU 270)"), the controller configured
- to partition the buffer memory into the plurality of independent buffers (see Hathaway et al. PAGE 4 [0056]: "buffer memory is divided into one or more partitions");

[The partitions are construed as the plurality of independent buffers as recited in the claims.]

- to configure the plurality of independent buffers into sets of buffers with at least one set having two or more buffers (see Hathaway et al. PAGE 4 [0057]: "Within each partition, a unique address or reference pointer is used to address a particular object entry"),

  [Object entries are construed as the two or more buffers as recited in the claims.]
- the sets of buffers matched to respective ones of a plurality of source-destination paths (see Hathaway et al. FIG 2: Port A, Port B, Port Z), and
- to provide circular-access for each set of one or more buffers such that an access to the last position in a particular set of one or more buffers (see Hathaway et al. FIG 14 and PAGE 7-8 [0114]: "FIG 14 describes a circular buffer containing object pointers (buffer memory addresses pointers). The pointers correspond to available (free) locations in the allocated partitions of buffer memory for a particular size object."),
- wherein each buffer of the plurality of independent buffers has a buffer size that is an integer power of two, to facilitate circular-access to the buffer, and (see Hathaway et al. PAGE 4 [0058]): "for a fixed buffer size 2^30 bytes").
- the controller is further configured to provide a write-interface (see FIG 2: 245) and a read-interface (see FIG 2: 255) to the application,
- the write-interface receiving, from the application, an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers to store the data (see Hathaway et al. PAGE 3 [0053]: "In general, an OMU (such as OMU 270) provides an object-addressable interface to the Controller or Processor via the control plane interface") and translating the identification of the select buffer to an address corresponding to the select buffer

(see PAGE 4 [0062]: "a descriptor is pointer to the address or addresses in memory containing the object"), and

- the read-interface receiving, from the application, the identification of the select buffer (see Hathaway et al. PAGE 3 [0053]: "In general, an OMU (such as OMU 270) provides an object-addressable interface to the Controller or Processor via the control plane interface"), and translating the identification of the select buffer to an address corresponding to the select buffer (see PAGE 4 [0062]: "a descriptor is pointer to the address or addresses in memory containing the object").

However, Hathaway et al. do not expressly disclose

- the controller is configured to partition the buffer memory into the plurality of independent buffers dependent upon a partition parameter received from the application that indicates the quantity of the plurality

In the same field of endeavor Nogradi discloses

- a controller operably coupled to the buffer memory (see FIG 2: 14 and COL 3 LINE 60: "Ethernet controller 14"), the controller configured to partition the buffer memory into the plurality of independent buffers (see FIG 1 and also COL 11 43-45: "The controller 14 reconfigures the shared memory") dependent upon a partition parameter (COL 11 LINES 37-41: 'using these new values') received from the application (see FIG 2: 32) that indicates a quantity of the plurality (see COL 4 LIENS 24-30),

It would have been obvious to modify the OMU of Hathway et al. to implement a controller to partition the memory based on a parameter received from the processor as taught by Nogardi.

The suggestion/motivation for doing so would have been for the benefit of smart buffer size adoptions feature (see Nogardi COL 2 LINES 27-39).

Therefore it would have been obvious to modify the OMU of Hathaway et al. to be a controller as taught by Nogardi for the benefit of a smart buffer size adaptation feature to arrive at the invention as specified in the claims.

As per claim 3, Hathaway et al. in view of Nogradi disclose

- wherein the buffer sizes of independent buffers are equal (see Nogradi COL 7 LINES 1-8).

As per claim 4, Hathaway et al. in view of Nogradi disclose the buffer management system of claim 1,

- wherein the controller is further configured to allocate the plurality of independent buffers among a plurality of source-destination paths (see Hathaway et al. FIG 2).

As per claim 7, a method of providing a plurality of independent buffers for use by an application, the method comprising:

- partitioning a memory buffer into the plurality of independent buffers (see Hathaway et al. PAGE 4 [0056]: "buffer memory is divided into one or more partitions"),

  [The partitions are construed as the plurality of independent buffers as recited in the claims.]
- wherein a size of each buffer of the plurality of independent buffers is an integer power of two, thereby facilitating circular-addressing within each buffer (see Hathaway et al. PAGE 4 [0058]): "for a fixed buffer size 2^30 bytes"),
- partitioning the plurality of independent buffers into sets of buffers (see Hathaway et al. PAGE 4 [0057]: "Within each partition, a unique address or reference pointer is used to address a particular object entry"),

[Object entries are construed as the two or more buffers as recited in the claims.]

- providing respective source-destination paths (see Hathaway et al. FIG 2: Port A, Port B, Port Z) with independent circular-access to each set of the sets of one or more buffers (see Hathaway et al. FIG 14 and PAGE 7-8 [0114]: "FIG 14 describes a circular buffer containing object pointers (buffer memory addresses pointers). The pointers correspond to available (free) locations in the allocated partitions of buffer memory for a particular size object.") and
- wherein at least one set of the sets of one or more buffers has two or more buffers (see FIG 14),
- providing a write-interface that receives, from the application, an identification of data to be stored and an identification of a select buffer of the plurality of independent buffers to store the data (see Hathaway et al. PAGE 3 [0053]: "In general, an OMU (such as OMU 270) provides an object-addressable interface to the Controller or Processor via the control plane interface"), translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored (see PAGE 4 [0062]: "a descriptor is pointer to the address or addresses in memory containing the object"), and providing a read-interface that receives, from the application, the identification of the select buffer (see Hathaway et al. PAGE 3 [0053]: "In general, an OMU (such as OMU 270) provides an object-addressable interface to the Controller or Processor via the control plane interface").

However, Hathaway et al. do not expressly disclose

- receiving, at a controller, a partition parameter from the application, partitioning a memory buffer into the plurality of independent buffers based on the partition parameter,

In the same field of endeavor Nogradi discloses

- a controller operably coupled to the buffer memory (see FIG 2: 14 and COL 3 LINE 60: "Ethernet controller 14"), the controller configured to partition the buffer memory into the plurality of independent buffers (see FIG 1 and also COL 11 43-45: "The controller 14 reconfigures the shared memory") dependent upon a partition parameter (COL 11 LINES 37-41: 'using these new values') received from the application (see FIG 2: 32) that indicates a quantity of the plurality (see COL 4 LIENS 24-30),

It would have been obvious to modify the OMU of Hathway et al. to implement a controller to partition the memory based on a parameter received from the processor as taught by Nogardi.

The suggestion/motivation for doing so would have been for the benefit of smart buffer size adoptions feature (see Nogardi COL 2 LINES 27-39).

Therefore it would have been obvious to modify the OMU of Hathaway et al. to be a controller as taught by Nogardi for the benefit of a smart buffer size adaptation feature to arrive at the invention as specified in the claims.

As per claim 8, Hathaway et al. in view of Nogradi disclose the method of claim 7,

- wherein the sizes of the plurality of independent buffers are equal (see Nogradi COL 7 LINES 1-8).

As per claim 9, Hathaway et al. in view of Nogradi disclose the method of claim 7,

- further including providing circular- addressing for each buffer, wherein the circular-addressing includes: incrementing an address to the buffer memory, and overwriting select bits of the address, corresponding to an index to the buffer within the buffer memory (see Hathawa et al. PAGE 8 [0015]).

As per claim 12, Hathaway et al. disclose an integrated circuit for providing a plurality of buffers for use by an application, the circuit comprising

- a buffer memory (see Hathaway et al. FIG 1: 250: Object Memory), and
- a controller that includes write control logic and read control logic (see Hathaway et al. PAGE 3 [0053]: "an OMU (such as OMU 270)"), wherein the controller is configured to
- partition the buffer memory into the plurality of buffers (see Hathaway et al. PAGE 4 [0056]: "buffer memory is divided into one or more partitions");

  [The partitions are construed as the plurality of independent buffers as recited in the claims.]
- to configure the plurality of independent buffers into sets of one or more of the independent buffers (see Hathaway et al. PAGE 4 [0057]: "Within each partition, a unique address or reference pointer is used to address a particular object entry"), and

  [Object entries are construed as the two or more buffers as recited in the claims.]
- to provide respective source-destination paths (see Hathaway et al. FIG 2: Port A, Port B, Port Z) with independent circular-access to each set of the sets of buffers and wherein at least one set of the sets of buffers has two or more buffers (see Hathaway et al. FIG 14 and PAGE 7-8 [0114]: "FIG 14 describes a circular buffer containing object pointers (buffer memory addresses pointers). The pointers correspond to available (free) locations in the allocated partitions of buffer memory for a particular size object."),
- each buffer of the plurality of buffers having a size that is an integer power of two (see Hathaway et al. PAGE 4 [0058]): "for a fixed buffer size 2^30 bytes"), and
- the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer (see FIG 14), and

- wherein the write control logic effects a storage of a data value to a select buffer of the plurality of buffers based on an identification of the data value and an identification of the select buffer (see Hathaway et al. PAGE 3 [0053]: "In general, an OMU (such as OMU 270) provides an object-addressable interface to the Controller or Processor via the control plane interface") by translating the identification of the select buffer into an address corresponding to the select buffer at which the data is to be stored (see PAGE 4 [0062]: "a descriptor is pointer to the address or addresses in memory containing the object"), and
- the read control logic effects a retrieval of the data value based on the identification of the select buffer (see PAGE 4 [0062]: "a descriptor is pointer to the address or addresses in memory containing the object").

As per claim 13, Hathaway et al. disclose the integrated circuit of claim 12,

- wherein the sizes of the plurality of buffers are equal (see Nogradi COL 7 LINES 1-8).

As per claim 14, Hathaway et al. disclose the integrated circuit of claim 12,

- wherein the use of each buffer as a circular buffer requires circular-addressing, and the controller is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory, and a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory (see Hathaway et al. PAGE 8 [0015]).

4. **CLAIM 2** rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway et al. (US PGPUB No. 20030061269) in view of Nogradi (US Pat No. 5947518) as applied to claim 1 above, and further in view of Catherwood et al. (US Pat No. 5249148).

As per claim 2, Hathaway et al. disclose the buffer management system of claim 1,

- wherein the controller is configured to include a circular-increment function, within a select buffer of the plurality of independent buffers, that requires only an address-increment function that increments bits of an address indicating the select buffer and a location within the select buffer (see Hathaway et al. PAGE 8 [0115]) and

However, Hathaway et al. does not expressly disclose

- a bit-overwrite function that overwrites bits of the address that differentiate the select buffer from others of the plurality of independent buffers while not overwriting bits that indicate the location within the select buffer to effect a circular-increment of a pointer to the location within the select buffer of the plurality of independent buffers.

In the same field of endeavor Catherwood et al. discloses a circular buffer addressing circuit comprising

- a bit-overwrite function that overwrites bits of the address that differentiate the select buffer from others of the plurality of independent buffers while not overwriting bits that indicate the location within the select buffer to effect a circular-increment of a pointer to the location within the select buffer of the plurality of independent buffers (see FIG 2 and COL 5 LINES 15-22).

It would have been obvious to modify Hatahway et al. to use a mask system of Catherwood et al. to implement the circular buffer addressing.

The suggestion/motivation for doing so would have been for the benefit of minimizing circuitry necessary to perform circular buffer addressing (see Catherwood et al. COL 2 LINES 50-55).

Therefore it would have been obvious to a person of ordinary skill in the art to modify Hatahway et al. to use the circular addressing of Catherwood et al. for the benefit of reduced circuitry to arrive at the invention as specified in the claims.

IV. ALLOWABLE SUBJECT MATTER

Claims 6, 11, and 16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

V. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Applicants' arguments filed 17 July 2008 have been fully considered.

Rejection of claims 1, 6, 7, 11, 12 and 16 as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309) is withdrawn.

Applicant's arguments, see Page 2, filed 17 July 2008, with respect to rejection of claims 1-4, 7-9, and 12-14 under Nogradi (US Pat No. 5974518) have been fully considered and are persuasive. The rejection of claims 1-4, 7-9, and 12-14 as being anticipated by Nogradi has been withdrawn.

RESPONSE TO AMENDMENTS/ARGUMENTS

With respect to the Applicants' representative's arguments concerning Nogradi, Examiner notes Nogradi is relied upon to teach partitioning the memory based on a parameter as recited in the claims. The limitations argued are mapped to Hathaway et al. (see above).

VI. CLOSING COMMENTS

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

VIa. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-4, 6-9, 11-14, 16 have received a fourth action on the merits and are subject of a final office action.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

VII. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin L. Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KLE/kp /KP/
27 September 2008

/Kevin L Ellis/
Acting SPE of Art Unit 2187